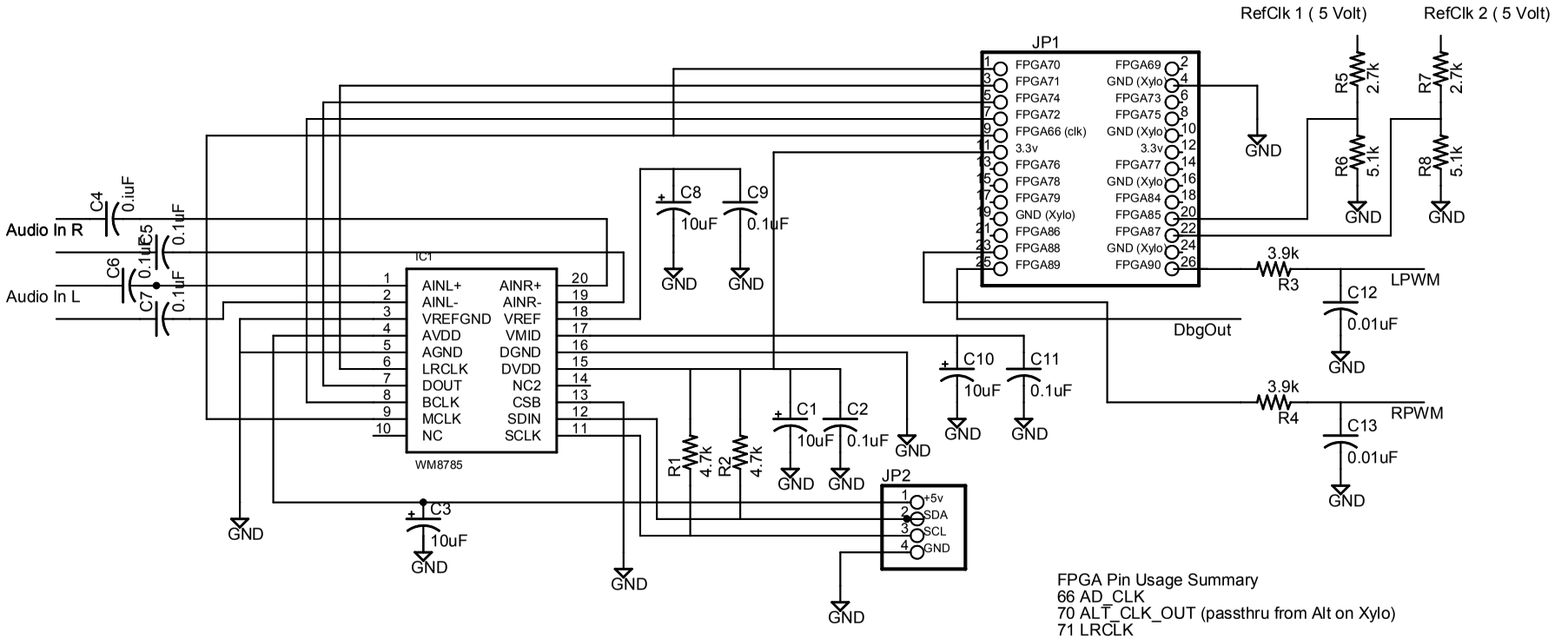

FPGA Pin Usage Summary
66 AD_CLK
70 ALT_CLK_OUT (passthru from Alt on Xylo)
71 LRCLK
72 BCLK
74 DOUT
85 CounteeClock (counted againt RefClock)
87 RefClk (1PPS or 10 khz)
88 Right PWM Out
89 Debug Out
90 Left PWM Out

Xylo - Wolfson Prototype (January 2006) VK6APH and KD5TFD	
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